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# HIGH SPEED LINEAR VARIABLE GAIN AMPLIFIER ARCHITECTURE

## FIELD OF THE INVENTION

This invention relates to amplifiers and in particular, amplifiers having variable gain, large bandwidth and low distortion.

## BACKGROUND OF THE INVENTION

Amplifiers are used to manipulate various signals within a circuit. The topology of the amplifier affects various operating aspects of the operating amplifier. For example, some amplifiers can deliver a high output current to a load. Other amplifiers can produce an output voltage swing that is approximately equal to the magnitude of the power supply of the amplifier circuit. Some amplifiers must provide an output with low cross-over distortion whereas other amplifiers are required to maintain gain and stability at high frequencies. These different requirements place constraints upon the design of the amplifier. It is often desirable

in an amplifier circuit to have variable gain, large bandwidth and low distortion. Conventional solutions use attenuators as front ends followed by high gain, closed-loop amplifiers or multiple lower gain closed-loop amplifiers. Disadvantageously, these conventional solutions require much higher FT (factor of ten) amplification to achieve these results.

## SUMMARY OF THE INVENTION

The present invention achieves technical advantages as a variable gain amplifier with wide bandwidth and low distortion by using two stages, a quad input stage with emitter degeneration and translinear current amplifier second stage.

The first stage quad configuration allows a constant DC output level. The output current of the quad is then fed into a resistance shunt current feedback amplifier with Darlington/level shift input stage to reduce transistor beta loading effects as well as allowing the largest dynamics out of the stage when a current to voltage and common mode feedback circuit are implemented in the same stage.

The second stage presents a low input impedance to the quad allowing optimization of the quad with minimize loss of bandwidth.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic circuit diagram of the present invention;

Figure 2 is a schematic of a conventional npn current feedback topology;

Figure 3 is a a simplified equivalent circuit shown in Figure 2; and

Figure 4 is a schematic circuit diagram of the translinear loop ($Q_{109}$ to $Q_{112}$) of the second stage of the present invention.

## DETAILED DESCRIPTION OF THE PRESENT INVENTION

The amplifier of the present invention, shown at 10 in Figure 1, is a combination of a quad 12 current drive circuit and a translinear current amplifier 14. The quad 12 provides a constant DC output level. As used herein, quad refers to a series-parallel configuration of four transistors. The quad is modified with emitter degeneration. The output drive current of the quad 12 is fed into the translinear current amplifier 14 comprising a resistive shunt current feedback amplifier with Darlington/level shift input stage. This arrangement reduces transistor beta loading effects as well as allowing the largest dynamics out of the stage when a current to voltage and common mode feedback circuit are implemented in the same stage. Translinear loop transistors 109 ("$Q_{109}$"), 110 ("$Q_{110}$"), 111 ("$Q_{111}$") and 112 ("$Q_{112}$") ensure a fast conveyence of the collector currents of $Q_{109}$ ("$Q_{C109}$") and $Q_{112}$ ("$Q_{C112}$") to the output. The current gain of the second stage is given as follows:

$$(IA_{out1} - IA_{out2})/(I_{out1} - I_{out2}) = (1+R_{123}/R_{124}) \cdot (I_{135}/I_{134}) \cdot (A/(1+A))$$

where $A = g_{mQ109} \cdot R_{124}$

The second stage 14 presents a low input impedance to the quad 12 allowing optimization of the quad 12 with minimum loss of bandwidth. Current to voltage conversion and common mode feedback implemented in the second stage 12 allows least delay, best distortion and highest bandwidth with such an architecture. The

inherent all npn core variable gain amplifier 10 ensures the best possible bandwidth and flexibility of use on both all npn or complementary bipolar processes.

The equations below better illustrate the operation of the second stage.

Figure 2 depicts a schematic of a conventional npn current feedback topology. From Figure 3, we can derive the transfer function of Figure 2. Figure 3 is the equivalent circuit of Figure 2.

$$\frac{I_{Q109}}{I_{in}}$$

1. $$\frac{V_{in} - V_{out}}{R_{123}} = I_{in} \rightarrow V_{in} = V_{out} + I_{in} \cdot R_{123};$$

2. $$\frac{V_{out}}{R_{124}} + I_{Q109} + \frac{V_{out} - V_{in}}{R_{123}} = 0;$$

$$I_{Q109} = g_{mQ109} \cdot V_{in}$$

3. $$V_{in} = \frac{I_{Q109}}{g_{mQ109}}.$$

Substituting equation (3) for equations (2) and (1) results in:

4. $$\frac{I_{Q109}}{g_{mQ109}} = V_{out} + I_{in}\ R_{123} \rightarrow V_{out} = \frac{-I_{Q109}}{g_{mQ109}} - I_{in} \cdot R_{123}$$

5. $$\frac{V_{out}}{R_{124}} + I_{Q109} + \frac{V_{out} - \frac{I_{Q109}}{g_{mQ109}}}{R_{123}} = 0$$

Substituting equation (4) for (5) and solving for $\frac{I_{Q109}}{I_{in}}$ provides as follows:

$$\frac{I_{Q109}}{I_{in}} = \frac{g_{mQ109}\,(R_{123} + R_{124})}{1 + g_{mQ109} \cdot R_{124}}$$

$$= \frac{(g_{mQ109} \cdot R_{124})}{1 + g_{mQ109} \cdot R_{124}} \quad \frac{(R_{123} + R_{124})}{R_{124}}$$

$$\frac{I_{Q109}}{I_{in}} = \frac{A}{1 + A}\left(1 + \frac{R_{123}}{R_{124}}\right) \text{ where } A = g_{mQ109} \cdot R_{124}$$

Referencing Figure 4, we can derive the transfer function for the translinear loop:

6. $$V_{be108} - V_{be112} + V_{be111} - V_{be110} = 0$$

$$V_{Tin}\left(\frac{I_{Q109}}{I_s}\right) - V_{Tin}\left(\frac{I_{Q112}}{I_s}\right) + V_{Tin}\left(\frac{I_{Q111}}{I_s}\right) - V_{Tin}\left(\frac{I_{Q110}}{I_s}\right) = 0$$

$$\frac{I_{Q109}}{I_{Q112}} \cdot \frac{I_{Q111}}{I_{Q110}} \rightarrow I_{Q109} \cdot I_{Q111} = I_{Q110} \cdot I_{Q112}$$

7. $$I_{Q109} + I_{Q112} = I_{134} \longrightarrow I_{Q112} = I_{134} - I_{Q109}$$

8. $$I_{Q110} + I_{Q111} = I_{135} \longrightarrow I_{Q111} = I_{135} - I_{Q110}$$

Substituting equation (7) and (8) for (6):

$$I_{Q109}\ (I_{135} - I_{Q110}) = I_{Q110}\ \ (I_{134} - I_{Q109})$$

$$(I_{Q109} \cdot I_{135}) - (I_{Q109} \cdot I_{Q110}) = (I_{Q110}\ I_{134}) - (I_{Q109} \cdot I_{Q110})$$

$$I_{Q109} \cdot I_{135} = I_{Q110} \cdot I_{134}$$

$$\frac{I_{Q110}}{I_{Q109}} = \frac{I_{135}}{I_{134}}$$

By combining the derivation of the transfer functions of Figure 3 and 4, we obtain:

$$I_{Q110} = I_{out} \rightarrow \frac{I_{out}}{I_{Q109}} = \frac{I_{135}}{I_{Q134}};$$

$$\text{Then}\ \ \frac{I_{out}}{I_{in}} = \frac{I_{out}}{I_{Q109}} \cdot \frac{I_{Q109}}{I_{in}}\ ;$$

$$\frac{I_{out}}{I_{Q109}} \cdot \frac{I_{Q109}}{I_{in}} = \frac{I_{135}}{I_{134}} \cdot \frac{T}{1+T}\left(1+\frac{R_{123}}{R_{124}}\right);$$

$$\text{Therefore :}\ \ \frac{I_{out}}{I_{in}} = \left(1+\frac{R_{123}}{R_{124}}\right)\left(\frac{R_{135}}{R_{134}}\right)\left(\frac{A}{1+A}\right) \text{where } A = g_m \cdot I_{Q109} \cdot R_{124}$$